Hestia-Power
Silicon Carbide MOSFET
Qualification Report

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Introduction

This qualification test report provides family-based qualification results of Hestia-Power Inc.(HPI)'s 650V, 1200V, 1700V SiC MOSFETs including bare die H1M065N*** and H1M120N*** series ; TO-247-3L packaged H1M065F*** and H1M120F*** series and TO-220-3L packaged H1M065B*** series. According to the results provided in this report and the generic data provided in previous qualification reports [1,2] the following parts are certified as qualified products. The qualification test methods are performed based on AEC-Q101 [3] or related JEDEC standards [4-8]. Before and after each qualification test, parameter verification is implemented as a minimum.

Bare Die	TO-247-3L	TO-220-3L
H1M065N020	H1M065F020	
H1M065N050	H1M065F050	H1M065B050
H1M065N100	H1M065F100	H1M065B100
H1M065N200	H1M065F200	H1M065B200
H1M120N030	H1M120F030	
H1M120N060	H1M120F060	
H1M120N120	H1M120F120	
H1M120N240	H1M120F240	
H1M170N1K0	H1M170F1K0	
H1M170N045	H1M170F045	

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Failure Criteria

A device failure is defined as the device does not satisfy the specifications of its data sheet or exhibit external damage attributed to the environment test.

Qualification Test Item

HPI's SiC MOSFETs were subjected to stress-test qualification items defined in AEC-Q101. These items are summarized in Table. 1.

Table 1. Qualification Test Items of HPI's SiC MOSFETs

Test Item	Test Condition	Reference
AC	T_A=121 °C, 100%RH, 2atm, 96hr	JESD22-A102
TC	-65 °C to 150 °C, 1000cycles	JESD22-A104
H3TRB	V_{DS}=100V, T_A=85 °C, 85%RH, 1000hr	JESD22-A10
HTRB	V_{DS}=80% of $V_{(BR)DSS}$, V_{GS}=0V, T_A=150 °C, 1000hr	JESD22-A108
HTGB+	V_{GS}=20V, V_{DS}=0V, T_A=150 °C, 1000hr	JESD22-A108
HTGB-	V_{GS}=-10V, V_{DS}=0V, T_A=150 °C, 1000hr	JESD22-A108
IOL	$\Delta T_j \geqq$ 100 °C, duration/cycles as indicated in AEC-Q101	MIL-STD-750 Method 1037
ESD-HBM	Classification at 25 °C	AEC-Q101-001
ESD-MM	Classification at 25 °C	AEC-Q101-002
ESD-CDM	Classification at 25 °C	AEC-Q101-005

V_{DS} : drain source voltage; V_{GS}: gate source voltage; T_A : ambient temperature; T_j := junction temperature

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Qualification Test Description and Result

Autoclave (AC)

Autoclave testing is used to determine the moisture resistance of non-hermetic packaged device. The device is subjected to highly humid atmosphere under pressure to force moisture into package. If there are weaknesses such as delamination and metallization corrosion, moisture can penetrate through the protective layer and leads to qualification failure.

Table 2. Autoclave Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
AC	H1M120F060	1200	Large (4.29 x 2.92)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 1
AC	H1M065F050	650	Large (4.29 x 2.92)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 1
AC	H1M120F240	1200	Small (2.32 x 1.73)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 2
AC	H1M120F120	1200	Medium (2.42 x 2.92)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 2
AC	H1M065B100	650	Medium (2.42 x 2.92)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 2
AC	H1M065B200	650	Small (2.32 x 1.73)	T_A=121 °C, 100%RH, 2atm, 96hr	0	77 x 1

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Temperature Cycle (TC)

Temperature Cycle testing is used to evaluate the ability of devices and solder interconnects when mechanical stresses are induces by alternating low- and high-temperature cycles. The coefficient of thermal expansion (CTE) mismatch between materials results in mechanical stresses and permanent changes in electrical and/or physical characteristics.

Table 3. Temperature Cycle Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
TC	H1M120F060	1200	Large (4.29 x 2.92)	-65 to 150 °C 1000cycles	0	77 x 1
TC	H1M065F050	650	Large (4.29 x 2.92)	-65 to 150 °C 1000cycles	0	77 x 1
TC	H1M120F240	1200	Small (2.32 x 1.73)	-65 to 150 °C 1000cycles	0	77 x 2
TC	H1M120F120	1200	Medium (2.42 x 2.92)	-65 to 150 °C 1000cycles	0	77 x 1
TC	H1M065F020	650	Very Large (4.29 x 5.38)	-65 to 150 °C 1000cycles	0	22 x 1**
TC	H1M065B200	650	Small (2.32 x 1.73)	-65 to 150 °C 1000cycles	0	77 x 1
TC	H1M120F120	1200	Medium (2.42 x 2.92)	-65 to 150 °C 500cycles	0	77 x 2
TC	H1M065B100	650	Medium (2.42 x 2.92)	-65 to 150 °C 500cycles	0	77 x 2

**Reduced sample size due to very large chip size. The sampling rate of a 22-samples per lot for the very large chip is similar to 77-samples per lot for the large chip.

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H3TRB

High humidity, high temperature reverse bias (H3TRB) testing is performed to determine the reliability of non-hermetic packaged device in humid environments. Temperature, humidity, and bias conditions are applied to accelerate the penetration of moisture through the external protective material and lead to moisture-related failure.

Table 4. H3TRB Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
H3TRB	H1M065F050	650	Large (4.29 x 2.92)	V_{DS}=100V, T_A=85 °C, 85%RH, 1000hr	0	77 x 1
H3TRB	H1M120F120	1200	Medium (2.42 x 2.92)	V_{DS}=100V, T_A=85 °C, 85%RH, 1000hr	0	77 x 1
H3TRB	H1M120F240	1200	Small (2.32 x 1.73)	V_{DS}=100V, T_A=85 °C, 85%RH, 1000hr	0	77 x 2
H3TRB	H1M065B200	650	Small (2.32 x 1.73)	V_{DS}=100V, T_A=85 °C, 85%RH, 1000hr	0	77 x 1
H3TRB	H1M065B100	650	Medium (2.42 x 2.92)	V_{DS}=100V, T_A=85 °C, 85%RH, 168hr	0	77 x 2

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HTRB

High temperature reverse bias (HTRB) testing is designed to evaluate the breakdown robustness of devices under high temperature and high electric field. The device is stressed at 80% rated drain source voltage ($V_{(BR)DSS}$) under high temperature which may result in early-life failure and field-accelerated failure.

Table 5. HTRB Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
HTRB	H1M120F060	1200	Large (4.29 x 2.92)	V_{DS}=960V, V_{GS}=0V, T_A=150 °C, 1000hr	0	77 x 2
HTRB	H1M065F050	650	Large (4.29 x 2.92)	V_{DS}=520V, V_{GS}=0V, T_A=150 °C, 1000hr	0	77 x 3
HTRB	H1M065F020	650	Very Large (4.29 x 5.38)	V_{DS}=520V, V_{GS}=0V, T_A=175 °C, 500hr*	0	77 x 1
HTRB	H1M120F030	1200	Very Large (4.29 x 5.38)	V_{DS}=960V, V_{GS}=0V, T_A=150 °C, 1000hr	0	22 x 1**
HTRB	H1M170F045	1700	Very Large (4.29 x 5.38)	V_{DS}=960V***, V_{GS}=0V, T_A=150 °C, 1000hr	0	22 x 1**
HTRB	H1M065B200	650	Small (2.32 x 1.73)	V_{DS}=520V, V_{GS}=0V, T_A=175 °C, 500hr*	0	77 x 1
HTRB	H1M065B100	650	Medium (2.42 x 2.92)	V_{DS}=520V, V_{GS}=0V, T_A=175 °C, 500hr*	0	77 x 1
HTRB	H1M065B050	650	Large (4.29 x 2.92)	V_{DS}=520V, V_{GS}=0V, T_A=175 °C, 500hr*	0	77 x 1

*equivalent to T_A=150 °C, 1000hr, according to AEC-Q101.

**Reduced sample size due to very large chip size. The sampling rate of a 22-samples per lot for the very large chip is similar to 77-samples per lot for the large chip.

*** 1700V Class MOSFETs are conditional released based on 960V HTRB results, due to the current limitation of DUT boards.

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HTGB

High temperature gate bias (HTGB) testing is designed to stress the gate oxide of MOS devices under the electric field imposed by the gate source voltage at high temperature. Both positive gate bias stress (HTGB+) and negative gate bias stress (HTGB-) were performed.

Table 6. HTGB+ Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
HTGB+	H1M120F060	1200	Large (4.29 x 2.92)	V_{GS}=20V, V_{DS}=0V, T_A=150 °C, 1000hr	0	77 x 1
HTGB+	H1M065F050	650	Large (4.29 x 2.92)	V_{GS}=20V, V_{DS}=0V, T_A=150 °C, 1000hr	0	77 x 1
HTGB+	H1M120F120	1200	Medium (2.42 x 2.92)	V_{GS}=20V, V_{DS}=0V, T_A=150 °C, 1000hr	0	77 x 1
HTGB+	H1M065F020	650	Very Large (4.29 x 5.38)	V_{GS}=20V, V_{DS}=0V, T_A=175 °C, 500hr*	0	22 x 1**
HTGB+	H1M120F030	1200	Very Large (4.29 x 5.38)	V_{GS}=20V, V_{DS}=0V, T_A=175 °C, 1000hr	0	22 x 1**
HTGB+	H1M120F120	1200	Medium (2.42 x 2.92)	V_{GS}=20V, V_{DS}=0V, T_A=175 °C, 1000hr	0	77 x 1
HTGB+	H1M170F1K0	1700	Very Small (1.36 x 1.34)	V_{GS}=20V, V_{DS}=0V, T_A=175 °C, 1000hr	0	77 x 1
HTGB+	H1M065B200	650	Small (2.32 x 1.73)	V_{GS}=20V, V_{DS}=0V, T_A=175 °C, 500hr*	0	77 x 1

*Equivalent to T_A=150 °C, 1000hr, according to AEC-Q101.

**Reduced sample size due to very large chip size. The sampling rate of a 22-samples per lot for the very large chip is similar to 77-samples per lot for the large chip.

Table 7. HTGB- Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
HTGB-	H1M065F050	650	Large (4.29 x 2.92)	V_{GS}=-10V, V_{DS}=0V, T_A=150 °C, 1000hr	0	77 x 3

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HTGB-	H1M120F240	1200	Small (2.32 x 1.73)	V_{GS}=-10V, V_{DS}=0V, T_A=175 °C, 500hr*	0	77 x 1
HTGB-	H1M065B200	650	Small (2.32 x 1.73)	V_{GS}=-10V, V_{DS}=0V, T_A=175 °C, 500hr*	0	77 x 1

*equivalent to T_A=150 °C, 1000hr, according to AEC-Q101.

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Intermittent Operating Life (IOL)

Intermittent Operating Life testing is used to accelerate the failure cause due to thermal mechanism. When the device is switched from zero bias to forward bias to achieve a variation in junction temperature (T_j) greater than 100℃, the coefficient of thermal expansion (CTE) mismatch between materials results in mechanical stresses and permanent changes in electrical and/or physical characteristics.

Table 8. IOL Test Results

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	Test Condition	Failure #	Sample # (size x lot)
IOL	H1M120F060	1200	Large (4.29 x 2.92)	$\Delta T_j \geqq 100\,^{o}C$, 2min/2min on/off, 15,000 cycles	0	77 x 1
IOL	H1M065F050	650	Large (4.29 x 2.92)	$\Delta T_j \geqq 100\,^{o}C$, 5min/5min on/off, 6000cycles	0	77 x 1
IOL	H1M065F100	650	Medium (2.42 x 2.92)	$\Delta T_j \geqq 100\,^{o}C$, 5min/5min on/off, 6000cycles	0	77 x 2
IOL	H1M120F240	1200	Small (2.32 x 1.73)	$\Delta T_j \geqq 100\,^{o}C$, 5min/5min on/off, 6000cycles	0	77 x 1
IOL	H1M065B200	650	Small (2.32 x 1.73)	$\Delta T_j \geqq 100\,^{o}C$, 5min/5min on/off, 3000cycles	0	77 x 1

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Electrostatic Discharge (ESD)

Electrostatic Discharge testing is implemented to evaluate the robustness of electrostatic charge accumulation. The source of electrostatic discharge is including of human body, robot arm, product packaging and so on.

Human Body Model (HBM)

Electrostatic Discharge - Human Body Model testing is used to simulate the electrostatic charge transfers from human body to devices through pin during manual device handling.

Machine Model (MM)

Electrostatic Discharge – Machine Model testing is used to simulate the electrostatic charge transfers from machine such as robot arm to devices. Due to machine usually made of metal, the electrostatic charge will through an extremely low resistance pass to devices.

Charged Device Model (CDM)

Electrostatic Discharge – Charged Device Model is used to simulate the electrostatic charge that accumulating in devices and discharge during manual device handling or pin grounding.

Table 9. ESD classifications

Test Item	Part #	Voltage (V)	Die Size (mm x mm)	HBM	MM	CDM	Class
ESD	H1M120F060	1200	Large (4.29 x 2.92)	±2000V	±400V	±1000V	HBM: H2 MM: M4 CDM: C5
ESD	H1M120F120	1200	Medium (2.42 x 2.92)	±1000V	±400V	±1000V	HBM: H1C MM: M4 CDM: C5
ESD	H1M120F240	1200	Small (2.32 x 1.73)	±500V	±400V	±1000V	HBM: H1B MM: M4 CDM: C5

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Table 10. Summary of qualification test results

Test Item	Total Sample Size	Failed Size	Results
Parameter Verification (PV)	4384	0	PASS
External Visual Inspection (EV)	4384	0	PASS
AC	693	0	PASS
TC	792	0	PASS
H3TRB	539	0	PASS
HTRB	737	0	PASS
HTGB+	506	0	PASS
HTGB-	385	0	PASS
IOL	462	0	PASS
ESD-HBM	90	N/A	Class H2~H1B
ESD-MM	90	N/A	Class M4
ESD-CDM	90	N/A	Class C5

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REFERENCE

[1] Hestia-Power JBS Gen-3 650V Qual Report ver.1.0.

[2] Hestia-Power JBS Gen-3 1200V Qual Report ver.1.0.

[3] AEC-Q101-C Automotive Electronics Council Rev.C.

[4] JESD22-A101 Steady State Temperature Humidity Bias Life Test

[5] JESD22-A102 Accelerated Moisture Resistance – Unbiased Autoclave

[6] JESD22-A104 Temperature Cycling

[7] JESD22-A108 Temperature, Bias, and Operating Life

[8] MIL-STD-750 Military Standard 750

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